REMARKS

Claims 1-14, 16-21 and 23-40 are pending. Claims 1-14, 16-21 and 34-40 have been allowed. Claims 23 and 27 have been amended. In view of the following, all of the claims are in condition for allowance. But if after considering this response the Examiner does not agree that all of the claims are in condition for allowance, then the Examiner is requested to schedule an interview with the Applicants' attorney to further prosecution of this application.

Rejection of Claims 23-26 Under 35 U.S.C. § 102(b) As Being Anticipated by Osawa et al. (US 5,946,247)

Claim 23

Claim 23, as amended, recites receiving a first address during a data-transfer cycle, generating a second address during the data-transfer cycle, and terminating the data-transfer cycle if the first address does not have a predetermined relationship to the second address.

For example, referring to FIGS. 3-5 and pages 5-11 of the present application, a comparator 18 compares a received external column address with an internal column address generated by a counter 14, and a column decoder 38 transfers data to/from a location of the array 30 residing at the internal column address. A control circuit 24 terminates this data-transfer cycle if the external column address does not have a predtermined relationship to the internal column address. For example, per the timing diagram of FIG. 3, the control circuit 24 may terminate the data-transfer cycle if the internal column address does not equal the external column address. It should be noted that this all occurs during a single data-transfer cycle t_{IPC}.

In contrast, Osawa does not disclose receiving a first address during a data-transfer cycle, generating a second address during the data-transfer cycle, and terminating the data-transfer cycle if the first address does not have a predetermined relationship to the second address. Instead, Osawa simply discloses a testing device for a memory (col. 20, lines 39-48; col. 45 - col. 48). This testing device is external to the memory, and has nothing to do with a memory itself that allows faster

data transfers during a read/write cycle. In fact, after reviewing Osawa in its entirety, the Applicants' attorney is unable to find any mention of a memory (or any other device) that performs all of the operations of claim 23 during a single data-transfer cycle as disclosed in the present application. Therefore, Osawa does not satisfy the limitations of claim 23.

Claims 24-26

Claims 24-26 are patentable by virtue of their dependency from independent claim 23.

Rejection of Claims 27-33 Under 35 U.S.C. § 102(e) As Being Anticipated by Tanaka (US 6,263,490)

Claim 27

Claim 27, as amended, recites generating a first address during a data-transfer cycle, and terminating the data-transfer cycle if the first address has a predetermined relationship to the predetermined value.

For example, referring to FIGS. 3-5 and pages 5-11 of the patent application, a column-address anticipation counter 14 generates an internal column (first) address and data is transferred to or from the location in the array 30 at the internal column address. A comparator 18 compares the internal column address to a predetermined value stored in the register/counter 16, and the control circuit 24 terminates the data-transfer cycle if the internal column address has a predetermined relationship (*e.g.*, is equal) to the value stored in the register/counter 16. It should be noted that this all occurs during a single data-transfer cycle t_{IPC}.

In contrast, Tanaka does not disclose generating a first address during a data-transfer cycle, and terminating the data-transfer cycle if the first address has a predetermined relationship to the predetermined value. Instead, Tanaka simply discloses an image processing apparatus (FIGS. 6-7; col. 4 - col. 5). A drawing circuit 18 performs such functions as "line drawing", "rectangular smearing", "rectangular transferring", "line drawing having patterns", "rectangular smearing having patterns", and "rectangular smearing and rectangular transferring being

accompanied with a raster operation" (col. 2, lines 21-26). The drawing circuit 18 produces a "drawing address" that is later compared to a "stop address", where both the drawing address and the stop address correspond to a pixel, not a memory storage location (col. 4). This has nothing to do with a memory that allows faster data transfers during a read/write cycle. In fact, after reviewing Tanaka in its entirety, the Applicants' attorney is unable to find any mention of a memory (or any other device) that performs all of the operations of claim 27 during a single data-transfer cycle as disclosed in the present application. Therefore, Tanaka does not satisfy the limitations of claim 27.

Claims 28-33

Claims 28-33 are patentable by virtue of their dependency from independent claim 27.

CONCLUSION

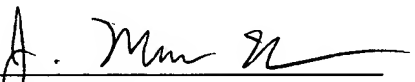
In light of the foregoing, all pending claims are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 08-2025.

If after considering this response the Examiner does not agree that all pending claims are in condition for allowance, the Examiner is requested to schedule an interview with the Applicants' attorney to further prosecution of this application.

DATED this 24th day of April 2006.

Respectfully Submitted,
GRAYBEAL JACKSON HALEY LLP



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